

Type No.: S5713N

Doc No.: KQC-B15698

2. Product outline

NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle.

Structure

Parameter	Specification	Unit
Number of pixels	256	--
Pixel height	2.5	mm
Pixel pitch	25	um
Photosensitive area length	6.4	mm
Package material	Ceramic	--
Window material	None *1	--

*1:When shipment, the outer of package is protected by tape.

3. Ratings and characteristics**3.1 Absolute maximum ratings** (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Value	Unit	Remark
Supply clock amplitude	V ϕ	15	V	
Operating temperature	Topr	-40 to +65	°C	No condensation
Storage temperature	Tstg	-40 to +85	°C	No condensation

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3.2 Electrical characteristics (Ta=25°C)						
Parameter		Symbol	Min.	Typ.	Max.	Unit
Video bias voltage *1		Vb	1.5	Vφ-3.0	Vφ-2.5	V
Saturation control gate voltage		Vscg	--	0	--	V
Saturation control drain voltage		Vscd	--	Vb	--	V
Start pulse voltage (φst) *1	High	Vφs(H)	4.5	Vφ	10	V
	Low	Vφs(L)	0	--	0.4	
Clock pulse voltage (φ1,2)	High	Vφ1,2(H)	4.5	5	10	V
	Low	Vφ1,2(L)	0	--	0.4	
Start pulse rise / fall time (φst)		trφs, tfφs	--	20	--	ns
Start pulse width (φst)		tpwφs	200	--	--	ns
Clock pulse rise / fall time (v1,2)		trφ1, trφ2 tfφ1, tfφ2	--	20	--	ns
Clock pulse width (φ1, φ2)		tpwφ1,2	200	--	--	ns
Start pulse (φst) and clock pulse (φ2) overlap		tφov	200	--	--	ns
Clock pulse space *2		X1,X2	trf-20	--	--	ns
Data rate *3		f	0.1	--	2000	kHz
Clock pulse line capacitance (φ1,2) at 8V bias		Cφ	--	27	--	pF
Saturation control gate line capacitance (Vscg) at 8V bias		Cscg	--	14	--	pF
Video line capacitance at 5V bias		Cv	--	10	--	pF
Video delay time *4		tvd	--	100	--	ns
Power consumption		P	--	--	1	mW

*1: V ϕ is input pulse voltage.

*2: trf is the clock pulse rise or fall time. A clock pulse space of "rise time / fall time -20" ns or more should be input if the clock pulse rise or fall time is longer than 20 ns.

*3: Vb=5.0V, V ϕ =8.0V

*4: Measured with C7883 driver circuit.

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3.3 Electro-optical characteristics (Ta=25°C, unless otherwise noted: Vb=2.0V, V ϕ =5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Photodiode dark current	ID	0.03	0.1	0.3	pA
Photodiode dark current *1	ID	0.1	0.25	0.375	pA
Photodiode dark output uniformity *2	ID	--	--	50	%
Photodiode capacitance	Cph	--	10	--	pF
Spectral response range (10% of peak)	λ	--	200 to 1000	--	nm
Peak sensitivity wavelength	λ_p	560	--	600	nm
Sensitivity @200nm	S200	45	--	120	mA/W
Sensitivity @250nm	S250	40	--	100	mA/W
Sensitivity @300nm	S300	55	--	130	mA/W
Sensitivity @400nm	S400	95	--	210	mA/W
Sensitivity @500nm	S500	165	--	290	mA/W
Sensitivity @600nm	S600	195	--	340	mA/W
Sensitivity @700nm	S700	185	--	330	mA/W
Sensitivity @800nm	S800	155	--	250	mA/W
Sensitivity @900nm	S900	70	--	130	mA/W
Sensitivity @1000nm	S1000	20	--	40	mA/W
Saturation charge	Qsat	22	25	--	pC
Saturation charge *1	Qsat	40	47	--	pC
Photo response non-uniformity (50% of saturation, excluding first and last elements) *3	PRNU	--	--	±3	%

*1: Vb=5.0V, V ϕ =10.0V

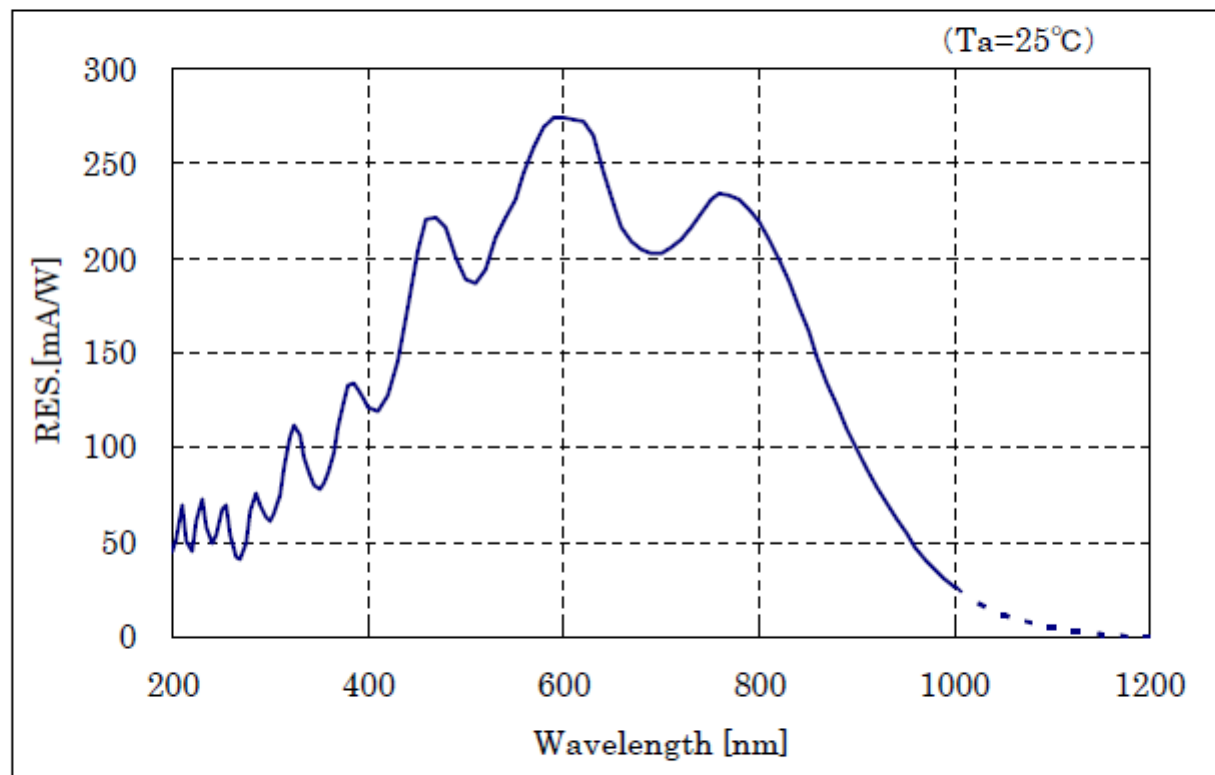
*2: Measured with Tec5 driver circuit

*3: 2856K, tungsten lamp

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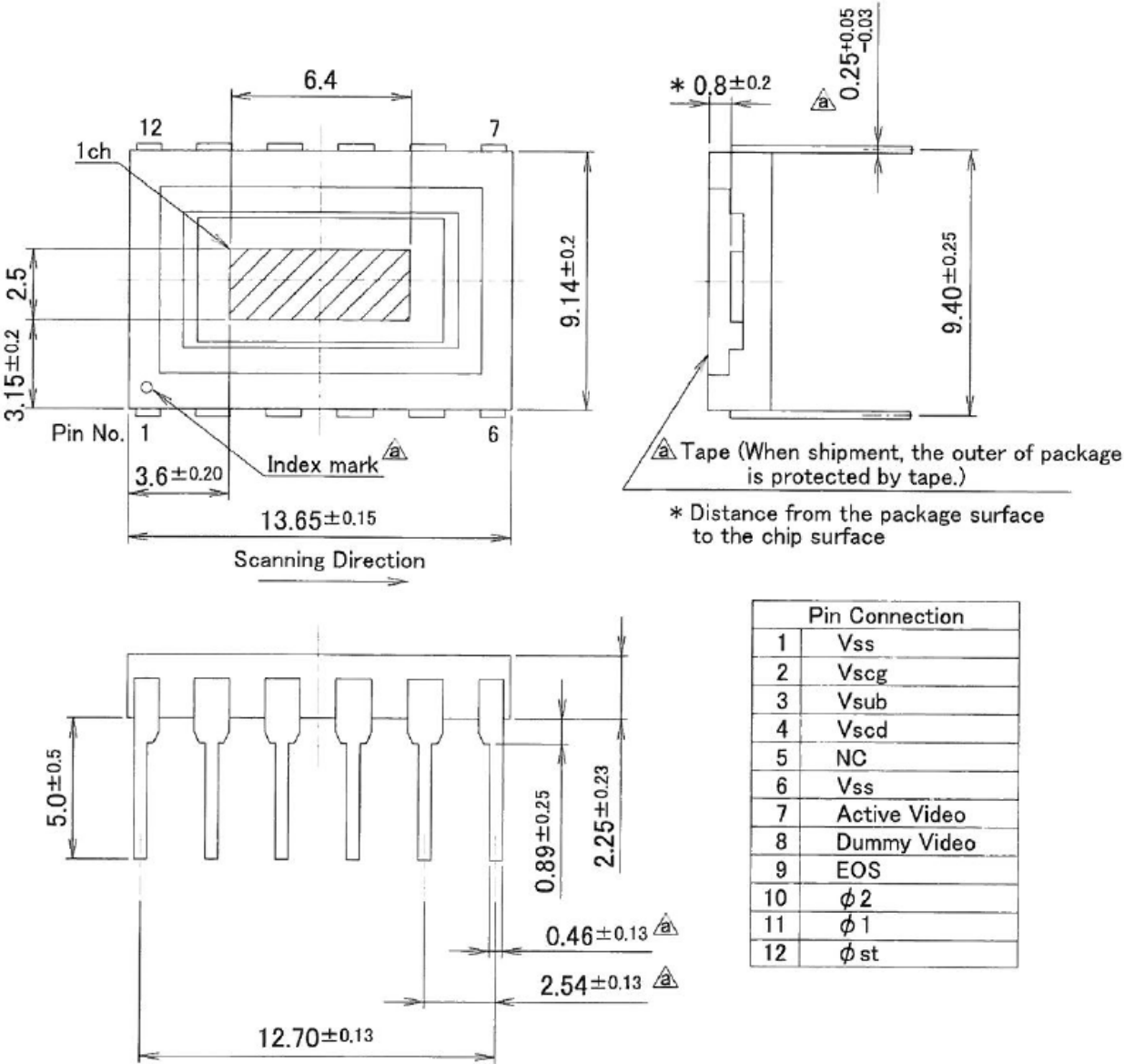
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3.4 Spectral response (example) *1



*1: Without window

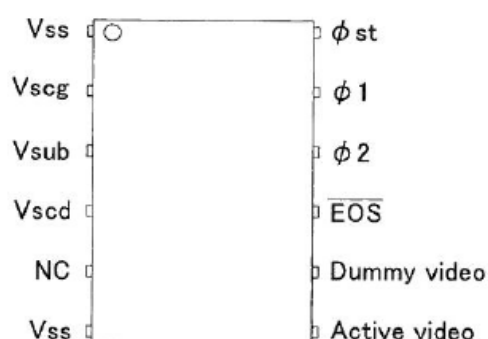
4. Dimensional outline (Unit : mm)



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5. Pin-out and recommended operating conditions



Vss, Vsub, and NC should be grounded.

Terminals	Input or output	Description
$\phi 1, \phi 2$	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained synchronized with the rise of $\phi 2$, the video data rate is equal to the clock pulse frequency.
ϕst	Input (CMOS logic compatible)	Pulse to start operation of the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
Vss	Passive node	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be set at the base line of each input pulse and is normally the ground level.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias at all times.
Active video	Output	Video output signal. A positive voltage should be applied to the video line which connects the photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of $\phi 1, \phi 2$ and ϕst is at 5V.
Dummy video	Output	This has the same structure as the active video, but is not connected to the photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. When in use otherwise, it should be open circuited.
Vsub	Passive node	Connected to the silicon substrate. This should be grounded.
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up to 5V using a 10 k Ω resistor. Negative polarity. The end of scan signal is obtained synchronized with $\phi 2$ right after the last photodiode is addressed.
NC		No connection. These should be grounded.

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6. Timing chart

